Add the new claims 15-47 as follows:

15. A semiconductor chip for optoelectronics, comprising:

an active thin-film layer in which a photon-emitting active zone is fashioned;

a carrier substrate for the thin-film layer that is arranged at a side of the thin-film layer facing away from an emission direction of the chip and is connected thereto; and

a plurality of mesas formed at the boundary between said carrier substrate and said active thin-film layer, said plurality of mesas being formed by at least one cavity formed in the active thin-film layer proceeding from the carrier substrate, said plurality of mesas being in a single light emitting diode.

16. A semiconductor chip according to claim 15, wherein a crossection of said at least one cavity becomes smaller over its course away from said carrier substrate.

17. A semiconductor chip according to claim 15, wherein said active thin-film layer includes a layer sequence based on In1-x-yAlxGayP (whereby $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq$ applies).

18. A semiconductor chip according to claim 15, wherein said at least one cavity is of such a depth that it parts said active zone.

19. A semiconductor chip according to claim 15, wherein said plurality of mesas are

formed only in radiation-generating regions of said active thin-film layers.

20. A semiconductor chip according to claim 15, wherein at least one trajectory of photons emitted by said active zone leads from a respective mesa to a neighboring one of said plurality of mesas.

21. A semiconductor chip according to claim 20, wherein said plurality of mesas taper toward said carrier substrate.

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22. A semiconductor chip according to claim 21, wherein said plurality of mesas have concave sidewalls.

23. A semiconductor chip according to claim 20, wherein said plurality of mesas are in a form of truncated pyramids.

24. A semiconductor chip according to claim 19, further comprising:

a cover layer, said active zone being in half of said plurality of mesas neighboring said cover layer.

25. A semiconductor chip according to claim 19, further comprising:

a cover layer which is transparent to a greatest degree for photons emitted by said active zone.

26. A semiconductor chip according to claim 25, wherein said cover layer is highly doped.

27. A semiconductor chip according to claim 18, further comprising:
a reflection layer covering said plurality of mesas.

28. A semiconductor chip according to claim 27, wherein said reflection layer includes a metallization layer underlaid with an insulating layer.

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29. A semiconductor chip according to claim 15, wherein said active thin-film layer has a thickness of between 5 μm and 50 μm.

30. A semiconductor chip according to claim 29, wherein said active thin-film layer is of a thickness of between 5 μm and 25 μm.

31. A semiconductor chip according to claim 15, wherein said at least one cavity has a depth that is greater than half a thickness of said thin-film layer.

32. A semiconductor chip according to claim 15, wherein said carrier substrate is electrically conductive, and further comprising:
an electrical contact area on a side of said carrier substrate facing away from said thin-film

layer.

33. A semiconductor chip according to claim 15, further comprising :

an electrical contact area next to said thin-film layer at that side facing toward said thin-film layer.

34. A semiconductor chip according to claim 15, further comprising:

an optical blooming coating on a surface of said thin-film layer lying opposite said carrier substrate.

35. A semiconductor chip according to claim 34, wherein said optical blooming coating is of silicon nitride.

36. A semiconductor chip according to claim 34, wherein said optical blooming coating is of conductive indium tin oxide.

37. A semiconductor chip according to claim 15, further comprising:

at least one contact location of said thin-film layer, said thin-film layer having no cavity in a region opposite said at least one contact location.

38. A semiconductor chip according to claim 15, wherein said plurality of mesas taper

in a direction toward said carrier substrate.

39. A semiconductor chip according to claim 38, wherein said plurality of mesas have a truncated pyramid-like or conical frustum-like shape and slanting sidewalls are at an angle of incidence φ of between 5° and 60°relative to a lateral extent direction of said thin-film layer.

40. A semiconductor chip as claimed in claim 39, wherein said slanting sidewalls are at an angle of incidence of between 10° and 40°.

41. A semiconductor chip according to claim 39, wherein said angle of incidence φ lies between 15° and 30°.

42. A semiconductor chip as claimed in claim 15, wherein said active layer has been epitaxially grown on a base substrate that is then removed.

43. A method for simultaneous manufacture of a plurality of semiconductor chips for optoelectronics having an active thin-film layer wherein a photon-emitting active zone (3) is formed, comprising the steps of:

epitaxially growing a layer sequence containing a photon-emitting zone on a growth substrate wafer;

forming at least one cavity in said layer sequence such that a plurality of mesas are formed in said layer sequence;

applying at least one insulating layer onto a surface of said layer sequence provided with cavities;

producing at least one through-contacting on said mesas;

applying a wafer composite including said growth substrate wafer and said layer sequence onto a carrier substrate wafer such that said mesas face toward said carrier substrate wafer, and

uniting said wafer composite with said carrier substrate wafer;

at least partially removing said growth substrate wafer;

applying an electrical contact onto that side of said layer sequence lying opposite said mesas; and

separating a wafer composite of said carrier substrate wafer and said structured layer sequence along parting tracks to form semiconductor chips, each of said semiconductor chips including a light emitting diode having a plurality of said mesas.

45. A method as claimed in claim 44, wherein said uniting step includes one of soldering and gluing.

46. A method according to claim 44, whereby said layer sequence is parted along said parting tracks before connecting said layer sequence to the carrier substrate wafer.

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47. A method according to claim 46, whereby said layer sequence is parted along said parting tracks in a separate step before said connecting step after removal of said growth substrate wafer and before said parting step of the carrier substrate wafer.